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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Sergey Art Unit : Unknown
Artamonov et al. Examiner : Unknown
Serial No.: 09/830,049
Filed : April 19, 2001
Title : PARALLEL PROCESSOR FOR MOTION ESTIMATOR

Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

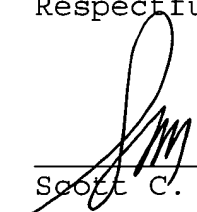
Applicant submits the references listed on the attached form PTO-1449, copies of which are enclosed.

This statement is being filed within three months of the filing date of the application or before the receipt of a first Office action on the merits. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: _____

6/15/01



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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 13109-002001	Application No. 09/830,049
Information Disclosure Statement (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Sergey Artamonov, et al.	
		Filing Date April 19, 2001	Group Art Unit

U.S. Patent Documents							
Examiner Initial	Design ID	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	4,897,720	1/30/1990	Wu et al.			
	AB	5,030,953	7/9/1991	Chiang			
	AC	5,453,799	9/26/1995	Yang et al.			
	AD	5,568,203	10/22/1996	Lee			
	AE	5,636,293	6/3/1997	Lin et al.			
	AF	5,719,642	2/17/1998	Lee			
	AG	5,512,962	4/30/1996	Homma			
	AH	5,594,813	1/14/1997	Fandrianto et al.			
	AI	5,619,268	4/8/1997	Kobayashi et al.			
	AJ	5,659,364	4/19/1997	Aoki et al.			
	AK						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Design ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL	0713339A2	5/22/1996	EPO				

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Design ID	Document
	AM	Komarek, K. et al. "Array Architectures for Block Matching Algorithms." <u>IEEE Trans. Circuits and Systems</u> 36 (1989): 1301-1308.
	AN	De Vos, L. et al. "Parameterizable VLSI Architectures for the Full-Search Block-Matching Algorithm." <u>IEEE Trans. Circuits and Systems</u> 36 (1989): 1309-1316.
	AO	Yang, K.-M. et al. "A Family of VLSI Designs for the Motion Compensation Block-Matching Algorithm." <u>IEEE Trans. Circuits and Systems</u> 36 (1989): 1917-1925.
	AP	Schiefer, P. "Picture Processing RAMs (PPRAMs) for Motion Estimation." <u>IEEE Trans. Consumer Electronics</u> 38 (1992): 570-575.
	AQ	De Greef, E. et al. "Mapping Real-time Motion Estimation Type Algorithms to Memory Efficient, Programmable Multi-Processor Architectures." <u>Microprocessing and Microprogramming</u> 41 (1995): 409-423.
	AR	Ackland, B.D. et al. "A Video-Codec Chip Set for Multimedia Applications." <u>AT & T Technical Journal</u> 72 (1993): 50-66.

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	